Supplementary Proposal
to the
Department of Energy
High Energy Physics Division
for Research and Development
for a Bottom Collider Detector
in FY 1990

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Summary

We seek **$248k** of supplemental funding in FY 1990 in support of the approved program of Fermilab T-784: research and development towards a hadron-collider detector dedicated to the physics of the B-meson system. Cost breakdowns by topic, and by institution, are given on p. 2, followed by discussion beginning on p. 3. An Appendix on p. 6 lists funding for BCD-related projects from the SSC.

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1. Workstations for detector simulation ($8k each to IIT, Iowa, Oklahoma, Penn, Princeton, Yale) $48k
2. Mechanical studies of the silicon vertex detector (Yale) $40k
3. Front-end readout for silicon strip detectors (Oklahoma) $40k
4. Data-collection chip for silicon strip detectors (Penn) $20k
5. Commercial electronic modules for the fixed-target test ($10k each to Penn, Princeton, Oklahoma, Yale) $40k
6. Detector supports for the fixed-target test (Iowa) $20k
7. Components for a prototype event-builder switch (Princeton) $40k

   Total **$248k**

We prefer that funds associated with items 2 and 7 be placed in a Fermilab User Account, but those for the other items would be more appropriate as direct supplements to the relevant university contract.

Total by Institution:

IIT $8k
Iowa $28k
Penn $38k
Princeton $58k
Oklahoma $58k
Yale $58k

Introduction

For two years a group, including the present authors, has been studying the possibility of constructing a new hadron-collider experiment with the goal of detailed measurements of CP violation in the B-meson system. This experiment might be performed at the Tevatron or at the SSC.

In October 1988 we submitted a Letter of Intent[1] to the Fermilab P.A.C. for a Bottom Collider Detector (BCD). They encouraged us to submit an R&D proposal, which we did on Jan. 2, 1989.[2] The first two phases of this proposal were approved as T-784, which forms the basis for the present funding request. Four topics are to be studied in the initial R&D program, which will culminate in a fixed-target beam test at Fermilab in 1990:

- Computer simulations of the proposed experiment.
- Development of a silicon-strip vertex detector capable of 3-dimensional vertex reconstruction.
- Development of a straw-tube tracking system to augment the vertex detector.
- Development of a high-speed data-acquisition system based on an event-builder switch.

Recent overviews of the BCD program are given in refs. 3 and 4.

In addition to the R&D program of T-784, members of the BCD collaboration are involved in several SSC Generic Detector Development Programs,[5−9] and several SSC Subsystem Proposals[10−16] (see also the Appendix on p. 6). With the exception of the program of ref. 9, the SSC programs and proposals are distinct from the parts of T-784 for which we seek support here.

The following 7 sections describe briefly the 7 items of the Supplemental Request as outlined on p. 2.

1. Detector Simulation

The Fermilab P.A.C. has indicated that the BCD collaboration should give high priority to extensive computer simulation of our proposed experiment. To achieve a detailed understanding of the detector in a realistic simulation, we are basing our work on the program GEANT. From partial simulations over the past year,[3,17,18] we estimate that a reasonably complete simulation will require about 500 MIPS of computing power. [While large, this is still quite small compared to the 1,000,000 MIPS we estimate to be needed to analyze the data from the experiment.]

The most cost-effective way of obtaining computing power at present is via UNIX workstations. Given the University Consortium pricing for DEC products (not available to Fermilab at this time), the DECstation 3100 workstation and an Imprimus 640 MByte hard disk can be purchased for approximately $8k, or about $1k per MIPS. This is very competitive with the price for a multiprocessor configuration from Silicon Graphics. The latter is favored by Fermilab, but is less suitable for distributed processing in the university environment.

One DECstation 3100 is now running GEANT at Princeton. We believe this is the first such workstation to do so.

We propose to purchase 6 additional DECstation 3100's at a cost of **$48k**. This would bring the computing power available to BCD to about 70 MIPS, or 15% of our eventual need for simulation, but adequate for the coming year.

2. Mechanical Studies of the Silicon Vertex Detector

Studies of a novel mechanical support structure for a silicon vertex detector have begun at Fermilab. Initial results[19] on the ability of a low-mass structure to dissipate 1 kWatt of heat are extremely encouraging. A scheme for assembly of the vertex detector out of self-supporting modules has been formulated.[20]

To continue these studies in 1990, we need **$40k** in equipment funds for glueing fixtures, a diamond saw, a small coordinate-measuring machine, a PC-clone computer, and upgrades to an existing wire-bonding/probe station.

3. Front-End Readout for Silicon Strip Detectors

The silicon vertex detector for the BCD requires a new generation of low-noise, low-power front-end electronics. In the past few months, specifications for such a new VLSI chip have been drawn up, based on the success of the so-called SVX and CAMEX chips. We now need to implement these specifications in prototype chips.

Towards this end we are fortunate that the U. Oklahoma collaboration with Oak Ridge Laboratory[6] can be enlarged to include work on the design of our 'BVX' chip. We request **$40k** to be used for prototype runs with the MOSIS foundry.

4. Data-Collection Chip for Silicon Strip Detectors

The BVX chip of item 3 resides on the silicon detectors. Each BVX chip processes 128 silicon strips. In the eventual vertex detector there might be as many as 10,000 such chips, too many for all to be read out directly. Rather we propose a data-collection chip that would buffer the data from 10 BVX chips. The 1000 data-collection chips would then be read out to the online computer.

In 1990 we wish to produce prototype quantities of this chip. The design work will be done at U. Pennsylvania. We request **$20k** for a foundry run to produce sample chips.

5. Commercial Electronic Modules for the Fixed-Target Test

We have the opportunity to test the prototype hardware being developed for T-784 in a test beam at Fermilab in Fall 1990. We have submitted a request to PREP at Fermilab for some $250k of electronics for this test. Of this, about $40k is not available, and requires new money. The missing items are primarily CAMAC crates and controllers, NIM bins, NIM coincidence circuits, and NIM gate generators – all basic, general purpose items.

We request **$40k** for purchase of these items, but we prefer this money **not** to go to PREP, but rather to the various participating universities. The practice of forming large equipment pools at the national laboratories has left the universities with almost no test equipment, and, as we see in the present case, only low-priority access to the pool for R&D projects.

6. Detector Supports for the Fixed-Target Test

In the fixed-target test several silicon strip detectors will be arrayed in configurations similar to those needed for use in a collider. The detector stands should have the ability to rotate the silicon wafers to study the effect of incidence angle on the detector performance. A design for this has been prepared at U. Iowa, whose implementation will require some **$20k** of machine-shop time.

7. Components for a Prototype Event-Builder Switch

Perhaps the most innovative idea associated with the Bottom Collider Detector is the event-builder switch,[9] which is based on the technology of a high-speed telephone exchange. This device will combine the multiple data streams off the detector, totalling about 1 MByte per event, into whole events at a rate of 10^5 events per second. This is four orders of magnitude faster than present capability, but will be essential for detectors in the SSC era.

A proposal[9] for design and simulation of an event-builder switch has been funded under the SSC Generic R&D program. The performance of a design for a 64-by-64 prototype switch has simulated using a commercial software package.

We seek **$40k** for the custom printed-circuit boards and components to construct a prototype switch. This prototype will be tested with simulated data as well as with other BCD detector prototypes in the Fermilab test beam.

Appendix
Funding for the Bottom Collider Detector in FY 1990 via SSC Programs

Funding for various R&D programs associated with the BCD has been forthcoming from the SSC as listed below. These funds are for issues of general interest to possible SSC experiments, and do not address the specific issues of Fermilab T-784 covered by the present Supplementary Proposal.

Funding via the SSC Generic Detector R&D Program:

1. **$40k** for evaluation of existing electronics for silicon strip detectors (*Yale.)*
2. **$50k** of equipment funds and **$80k** operating funds for design and simulation of a barrel-switch event builder (*Fermilab*).
3. **$65k** for studies of silicon drift chambers (*Princeton*).
4. **$90k** (tentative) for studies of radiation damage to silicon vertex detectors (*Oklahoma*).

Funding via the SSC Subsystem R&D Program:

1. **$135k** for development of a straw-tube tracking subsystem (*Princeton*).
2. **$450k** for development of silicon pixel detectors (*LBL* and *Hughes Aircraft*, but no funding directly to the BCD collaboration).
3. **$30k** for development of silicon drift chambers (*Princeton*).

The following three Subsystem proposals were not funded by the SSC, in part because the technologies are of interest only to the BCD among possible SSC experiments.

4. Studies of a trigger processor based on a parallel computer farm (*Penn*).
5. Development of detectors for identification of pions, kaons and protons.
6. Development of a silicon strip vertex detector.

References

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4. BCD Collaboration, *The Bottom Collider Detector*, to appear in the Proceedings of the 1989 Breckenridge Workshop on Physics at Fermilab in the 1990's.
5. S. Dhawan *et al.*, *Performance Limits of Silicon Strip Front-end Electronics for the SSC Bottom Detector*; *Mechanical Structures for Microvertex Detectors*.
6. G.R. Kalbfleisch *et al.*, *A Proposal to Investigate Radiation Hardened Semiconductor Device Technologies for Use with Silicon Strip Detectors at the SSC*.
7. C. Lu *et al.*, *Proposal for Generic Detector Development in FY 1990* (Silicon Drift Chambers).
8. E. Barsotti *et al.*, *Proposal for Generic Detector R&D for the SSC* (Processor Farms).
9. E. Barsotti *et al.*, *Proposal for Generic Detector R&D for the SSC* (Event Builder).
10. M.S. Alam *et al.*, *A Microvertex Detector for B-Physics at the SSC*.
11. J.F. Arens *et al.*, *SSC Detector R&D Proposal: Development of Technology for Pixel Vertex Detector*.
12. C. Lu *et al.*, *Proposal to the SSC Laboratory for Research and Development of a Straw-Tube Tracking System*; also, *Prototype Studies of the Straw Tube Proportional Chamber*, Princeton U. preprint DOE/ER/3072-56 (Dec. 7, 1989).
13. A.T. Goshaw *et al.*, *A Proposal for Research and Development of a Hybrid Central Tracking Chamber for the SSC*.
14. W. Chen *et al.*, *SSC Detector Subsystem R&D Proposal to Develop Track and Vertex Detector Based on Silicon Drift Devices*.
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18. N.S. Lockyer, *B Factory with Hadron Colliders*, U. Penn preprint UPR-0175e, to appear in the Proceedings of the 1989 KEK Topical Conference on e^+e^- Collision Physics.
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20. C. Lindenmeyer, *Proposed Method of Assembly for the BCD Silicon Strip Vertex Detector Modules*, Fermilab TM-1627 (Oct. 16, 1989).